

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	"6714902"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/07/20 13:20
L2	15	("4527249" "4722071" "4924430" "5095454" "5191541" "5355321" "5600787" "5648909" "5657239" "5805459" "5946475" "6026222" "6086626" "6097884" "6286126").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/07/20 14:00
L3	768	feedback near cycle	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/07/20 14:00
L4	547	L3 and @ad<"20010901"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/07/20 14:03
L5	0	L4 and 7%%/\$.ccls.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/07/20 14:02
L6	513	L3 and @ad<"20010901"	US-PGPUB; USPAT	OR	OFF	2005/07/20 14:03
L7	153	L6 and sensiti\$6	US-PGPUB; USPAT	OR	OFF	2005/07/20 14:06
L8	720	714/738.ccls.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/07/20 14:08
L9	604	L8 and @ad<"20010901"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/07/20 14:09
L10	427	L9 and (cycl\$2 or loop\$1 or feedback or sequential)	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2005/07/20 14:10
L13	8	"5910958"	USPAT	OR	OFF	2005/07/20 15:14
L14	7	("5910958").URPN.	USPAT	OR	OFF	2005/07/20 15:23
L15	35	(boolean adj satisfiability) and @ad<"20010901"	USPAT	OR	OFF	2005/07/20 15:23



Welcome United States Patent and Trademark Office

☐ Search Results

BROWSE

SEARCH

IEEE XPLORE GUIDE

Results for "(larrabee<in>au) <and> (test pattern generation<in>ti)"

Your search matched 4 of 1194402 documents.

e-mail

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

» Search Options

[View Session History](#)
[New Search](#)

Modify Search

>>

☐ Check to search only within this results set
Display Format: ☒ Citation ☐ Citation & Abstract

» Key

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

Select Article Information

- ☐ 1. **Test pattern generation using Boolean satisfiability**
Larrabee, T.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
Volume 11, Issue 1, Jan 1992 Page(s):4 - 15
Digital Object Identified 10.1109/43.108614
[AbstractPlus](#) | Full Text: [PDF](#)(972 KB) IEEE JNL
- ☐ 2. **A framework for evaluating test pattern generation strategies**
Larrabee, T.;
Computer Design: VLSI in Computers and Processors, 1989. ICCD '89. Proceed
IEEE International Conference on
2-4 Oct. 1989 Page(s):44 - 47
Digital Object Identified 10.1109/ICCD.1989.63325
[AbstractPlus](#) | Full Text: [PDF](#)(292 KB) IEEE CNF
- ☐ 3. **Test Pattern Generation for Realistic Bridge Faults in CMOS ICs**
Ferguson, F.J.; Larrabee, T.;
Test Conference, 1991, Proceedings., International
26-30 Oct 1991 Page(s):492
[AbstractPlus](#) | Full Text: [PDF](#)(500 KB) IEEE CNF
- ☐ 4. **Test pattern generation for current testable faults in static CMOS circuits**
Ferguson, F.J.; Larrabee, T.;
VLSI Test Symposium, 1991. 'Chip-to-System Test Concerns for the 90's', Dig
15-17 April 1991 Page(s):297 - 302
Digital Object Identified 10.1109/TEST.1991.208174
[AbstractPlus](#) | Full Text: [PDF](#)(444 KB) IEEE CNF

 Indexed by
 Inspec

[Help](#) [Contact Us](#) [Privacy &](#)

© Copyright 2005 IEEE -



Welcome United States Patent and Trademark Office

☐ Search Results

BROWSE

SEARCH

IEEE XPLORE GUIDE

Results for "(boolean satisfiability<and>cyclic) <and> (pyr >= 1951 <and> pyr <= 2001)"

Your search matched 8 of 1194402 documents.

e-mail

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

» Search Options

[View Session History](#)
[New Search](#)

Modify Search

(boolean satisfiability<and>cyclic) <and> (pyr >= 1951 <and> pyr <= 2001)

>>

☐ Check to search only within this results set
Display Format: ☒ Citation ☐ Citation & Abstract

» Key

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine


IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

Select Article Information

- ☐ 1. **Hazard-free implementation of speed-independent circuits**
 Kondratyev, A.; Kishinevsky, M.; Yakovlev, A.;
 Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
 Volume 17, Issue 9, Sept. 1998 Page(s):749 - 771
 Digital Object Identified 10.1109/43.720313
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(600 KB) IEEE JNL
- ☐ 2. **IGRAINE-an Implication GRaph-bAsed engine for fast implication, justifi propagation**
 Tafertshofer, P.; Ganz, A.; Antreich, K.J.;
 Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
 Volume 19, Issue 8, Aug. 2000 Page(s):907 - 927
 Digital Object Identified 10.1109/43.856977
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(660 KB) IEEE JNL
- ☐ 3. **An efficient heuristic approach to solve the unate covering problem**
 Cordone, R.; Ferrandi, F.; Sciuto, D.; Calvo, R.W.;
 Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction:
 Volume 20, Issue 12, Dec. 2001 Page(s):1377 - 1388
 Digital Object Identified 10.1109/43.969431
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(263 KB) IEEE JNL
- ☐ 4. **Symbolic simulation techniques-state-of-the-art and applications**
 Blank, C.; Eveking, H.; Levihn, J.; Ritter, G.;
 High-Level Design Validation and Test Workshop, 2001. Proceedings. Sixth IE
 7-9 Nov. 2001 Page(s):45 - 50
 Digital Object Identified 10.1109/HLDVT.2001.972806
[AbstractPlus](#) | Full Text: [PDF](#)(117 KB) IEEE CNF
- ☐ 5. **A decision procedure for bit-vector arithmetic**
 Barrett, C.W.; Dill, D.L.; Levitt, J.R.;
 Design Automation Conference, 1998. Proceedings
 15-19 Jun 1998 Page(s):522 - 527
[AbstractPlus](#) | Full Text: [PDF](#)(604 KB) IEEE CNF
- ☐ 6. **Using reconfigurable computing techniques to accelerate problems in the case study with Boolean satisfiability**
 Peixin Zhong; Ashar, P.; Malik, S.; Martonosi, M.;
 Design Automation Conference, 1998. Proceedings
 15-19 Jun 1998 Page(s):194 - 199
[AbstractPlus](#) | Full Text: [PDF](#)(588 KB) IEEE CNF

- ☐ 7. **Robust encodings in genetic algorithms: a survey of encoding issues**
Ronald, S.;
Evolutionary Computation, 1997., IEEE International Conference on
13-16 April 1997 Page(s):43 - 48
Digital Object Identified 10.1109/ICEC.1997.592265
[AbstractPlus](#) | Full Text: [PDF](#)(668 KB) IEEE CNF
- ☐ 8. **Some recent advances in software and hardware logic simulation**
Murgai, R.; Fujita, M.;
VLSI Design, 1997. Proceedings., Tenth International Conference on
4-7 Jan. 1997 Page(s):232 - 238
Digital Object Identified 10.1109/ICVD.1997.568081
[AbstractPlus](#) | Full Text: [PDF](#)(648 KB) IEEE CNF
- 

Indexed by

 Inspec[Help](#) [Contact Us](#) [Privacy &](#)

© Copyright 2005 IEEE -